EPIC Members Event Report

Meet or eat? Collaboration and/or Competition in Photonic Integrated Circuits?

Rüschlikon (Zurich), Switzerland
5-6 December 2013

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Article originally submitted to

electro optics

http://www.electrooptics.com/news/news_story.php?news_id=2024

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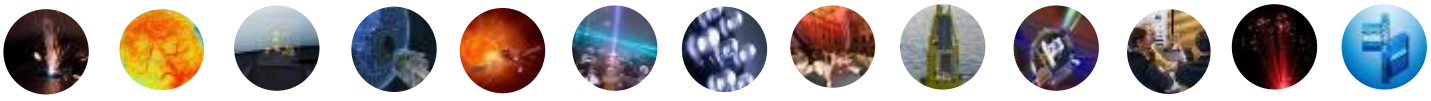
About the EPIC Members Event Reports

Initiated by the founder of EPIC Dr. Thomas Pearsall in 2003, these reports are prepared by members of EPIC to the benefit of the wider community. If you did not have a chance to attend the event but would like to know some key highlight, this report is for you. Emphasis is placed on exploring technical and business opportunities for the members of EPIC.



On 5-6 December 2013, a workshop organized by EPIC (European Photonics Industry Consortium) took place under the title: “Meet or eat? Collaboration and/or competition in photonic integrated circuits”. The event was hosted by IBM Research GmbH in Rüschlikon, close to Zurich, in Switzerland. More than 80 participants, mostly from industry, discussed the current status and challenges in integrated photonics. Already in the 90’s, so almost 20 years ago, integrated photonics received a lot of attention and was deemed to solve the challenges in increasing the bandwidth demand. With the burst of the telecom bubble early 2000, a substantial part of the emerging technology vanished but some integration technologies are presently emerging again the most important ones being silicon photonics, III-V photonics and dielectric waveguide technology. And combinations of these technologies seem to become increasingly important.

Silicon photonics is a good example. It is viewed as the ideal platform to take advantage of the mature infrastructure of the CMOS industry, combine electronics with photonics and scale up production at low cost. But what about the III-V semiconductor based photonic platforms? And how will this technology be integrated in a system? Would it be better to combine the glass, III-V and silicon integrated optic technologies into one platform?

Clearly, despite all the integration efforts, the photonics industry is far from the level of integration and standardized assembly as we know it from electronics.

Complex electrical chips are interconnected at system level through thousands of signals applying just a few assembly steps. Why is it so hard to make even relatively simple integrated optic devices successful, such as fiber to the home (FTTH) transceivers.

The volume is there, the enabling technology, like Indium Phosphide, as well. But the labor cost of a hybridly assembled FTTH transceiver is negligible and its performance is hard to beat. New technologies have to make a difference and the customer only cares about performance and cost. Coherent receivers are a positive example in this respect, the integrated solution provides stability and so a performance advantage.

Three integrated optic platforms were discussed in more detail; silicon photonics, III-V materials (especially Indium Phosphide) and glass on silicon (silica/PLC) and Silicon Nitride or TripleX. All have their specific advantages, and their combinations may bring the solution to bridge deficiencies. Glass waveguides may be used for ultra-low loss optical delay lines. Silicon's best advantage was recognized to be its compactness and theoretical compatibility with CMOS electronics. Additionally, the hybrid or heterogeneous integration of III-V on silicon has been investigated extensively with the goal to integrate lasers into a silicon photonics chip. While several integration models may be viable, it is clear that a combination of materials is required to gather all required electrical and optical functions in one platform. The other extreme is that everything is done in silicon except for those functions where silicon cannot deliver.

The atmosphere inspired a constructive, collaborative and open-minded dialogue

Worldwide experts from leading organizations meet to discuss opportunities in photonic integrated circuits

Another question that was addressed is whether it is better to use die-level hybrid integration of III-V chips with silicon chips or rather bonding-based heterogeneous integration of III-V thin films onto silicon. While the potential opportunities of the heterogeneous integration were recognized in terms of cost or performance, most experts emphasized that the industrial challenges to develop the industrial supply chain for this approach are still considerable.

Device testing is an important aspect of establishing and optimizing integrated optic technologies. Optical and electro-optical characterization is time consuming. Hence, it is an important cost aspect and may even limit the production capability, even more than the throughput of the wafer processing tools. Besides device test, also the packaging is a dominating factor in the overall product cost. As all integrated optic platforms have a need for a packaging solution, one may think of a common approach benefiting them all. Standardization is an important aspect to drive such a development, andEPIC could play a role here.

While all participants agreed that packaging is an important issue requiring new low cost and scalable solutions, opinions diverged on the approaches to be pursued. Passive or visual alignment approaches appear simpler as one does not have to 'power' the components to be aligned. But active alignment relaxes the accuracy requirements of the components and may lead to better results.

As a consequence of this discussion, it was proposed to devote the next workshop to test, assembly and packaging.

The participants had the opportunity to tour in small groups the IBM Research facilities

A video of the event is available on www.youtube.com/watch?v=k2nDd9dNBak

EXTRA: AVAILABLE TO MEMBERS OF EPIC

The presentations made at the workshop, and all events organized by EPIC, are available at no cost to members

Several networking opportunities allowed the attendees to discuss more in detail

The event was organized by EPIC and attended by 80 invited industry experts and leaders