

EPIC Technology Workshop on Photonic Integrated Circuits Packaging Standardization

's-Hertogenbosch, The Netherlands

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Hosted by TE Connectivity



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About the EPIC Members Event Reports

Initiated by the founder of EPIC Dr. Thomas Pearsall in 2003, these reports are prepared by members of EPIC to the benefit of the wider community. If you did not have a chance to attend the event but would like to know some key highlight, this report is for you. Emphasis is placed on exploring technical and business opportunities for the members of EPIC.



Don't fit the package to the chip, fit the chip to the package

More than 50 of the key players in the coming market for packaging of photonic integrated circuits shared their views and thoughts in the workshop organized by EPIC under the name of "Photonic Integrated Circuits Packaging and Standardization" hosted by TE Connectivity in 's-Hertogenbosch (The Netherlands) on 18-19 of June 2014. The attendance list brought together an impressive lineup with participants from: *Adamant, ADVA Optical Networking, AIFOTEC, ALT, BASF Coatings, BESI, Boschman Technologies/APC, CEA-LETI, CMC Microsystems, Corning, Eindhoven University of Technology, Entroptix, EPIC, ficonTEC, Finetech, Fraunhofer HHI, greenTEG AG, HAT Lab, Huawei (Caliopa), Huawei European Research Center, IBM, III-V lab, Infineon, Karlsruhe Institute of Technology (KIT), LioniX, Lovalite, Multiphoton Optics, Nanium, Oclaro, OneChip Photonics, Opticap, Panda, Phoenix Software, PI miCos, PNO, Prysmian Group, SATRAX, Sencio, Southampton University, SQS, Sumitomo Bakelite, TE Connectivity, Technobis ipp, Tyndall, University of Paderborn, US Conec, VTT, XiO Photonics, Xyratex and Yelo.*



It is by now quite commonly accepted by the Photonics community that the future of system in a package (SiP) products fully depends on the technology evolution of PICs. The key selling point for PICs is that they allow electro-optical systems to be more compact and offer higher performance as well as potential lower cost than those resulting of the integration of discrete components. During the last decade, the key technology platforms for the realization of PICs, namely Silicon Photonics, Indium Phosphide (InP) and

TripleX, have been developed to the extent that they are already globally used in an increasing number of applications with an ever increasing functionality according to Moore's law. It is important to notice that the new enabled market products do not only stem from the big companies (IBM, Intel, TE Connectivity etc.) but are also developed by SMEs. It is the latter where the PIC technology encounters one of the major hurdles: the lack of low cost standardized packaging concepts both for testing purposes as well as for the low, medium, and high volume production of application specific SiP products.

The most important aim of the workshop was to bring together members from different parts of the supply chain and to start a discussion that could lead to agreements which will become the stepping stone for those standards. The most important aspects of the discussion were two-fold: (1) the need for a change of mentality in which the PIC designer should aim to fit their designs to standard packages and not developing an optimized design with the need for completely customized and, thus, expensive package; and (2) the evaluation of the need for a hermetically sealed package, which in some applications increases cost without bringing enough added value to the system.

The workshop started with setting up of the scene session. Carlos Lee, General Director of EPIC, opened with the statement on 5000 photonic companies and 40 photonic clusters currently operating in Europe. It is important to notice that the niche market characteristic of photonics as a key enabling technology is evidenced by the fact that around 40% of those companies have been established in the last 10 years. This is indeed one of the reasons why despite all the integration efforts, the photonics industry is far from the level of integration and standardized assembly as we know it from the more mature electronics counterpart. The floor was afterwards taken by Andy Longford, CEO of Panda, who did an excellent job defining the 6 levels of packaging, namely Level 0 Gate to gate interconnections within the PIC, Level 1 the connection between the chip to its package,

Level 2: Printed circuit board, from component to component or to external connector, Level 3: connections between PCBs including backplanes and motherboards, Level 4: connections between subassemblies, for example a rack and level 5: connections between physically separated systems. This classification helped to set a common language, as in previous events the expression “photonic packaging” was used with different meanings and leading to miscommunication. In addition, the MEMS and electronics packaging status were brilliantly presented as an example of more standardized packaging technologies. The floor was followed by Bob Musk, CEO of Entroptix, who gave a very interesting overview of the history of packaging of optoelectronic devices over the last 30 years. Of special interest was the enumeration of some of the key challenges for the packaging of PICs, such as the difficulty of the distribution of the RF contacts around the chip, the fragile characteristic of InP chips and the heat dissipation.

At this point the discussion took an interesting turn, as the common agreed solution for the problems enumerated by Mr Musk was to continue with the ongoing change of mentality of the photonic designers of fitting their designs to standard packages optimum for either testing or application specific, which in some case have to be hermetic, such as for instance as in most ESA applications (European Space Agency).



22 presentations by industry, research organizations, projects. 50 participants.

Is the current TRL (Technology Readiness Level) of PICs high enough to consider that packaging is the present bottleneck?

The answer to the question above was a major “yes”, as evidenced by the presentations of some of the key representatives of the manufacturing of the 3 key PIC technologies in Europe, Mike Wale, Director at Oclaro, and manufacturer of InP PICs, Arne Leinse, Vice-President at LioniX, the manufacturer of TripleX technology and Timo Aalto, Research Team Leader at VTT, representative of the ePIXfab consortium, as the leading Silicon Photonics platform for the manufacturing of Silicon Photonics in Europe. The presentation of Michael Lebby, CEO OneChip, and the constructive discussion started afterwards were a clear evidence that now is the time for PICs to focus on solving their current packaging issues. Mr. Lebby, coming from the US, was very impressed by the activities in Europe in PIC technology, and especially in the PARADIGM project. Bob Musk presented the packaging activities within PARADIGM, which is an FP7 funded project with the aim of creating a dramatic reduction of fabrication, packaging and testing costs as well as the development time of Application Specific PICs (ASPICs) based InP by bringing a generic, and thus, application independent approach. That “paradigm” of using generic technologies to satisfy very different applications was very much highlighted by Michael Lebby. But despite the good position that Europe has on the development of PICs, during the discussion it was concluded that in the current status, the main technology users and manufacturers were still working on their own proprietary solutions, and that was the reason for the relatively slow move of the device manufacturers from the integration of discrete components to PICs.

The ePIXfab packaging technology was presented by Nicola Pavarelli, research scientists at Tyndall, and Stéphane Bernabe Optical Packaging Engineer at CEA-LETI. ePIXfab, in the framework of the FP7 project ESSenTIAL, is currently dealing with the commercial take-up of Silicon Photonics.

In addition, the potential for TripleX technology not only as a competing PIC technology but as a potential enabler of low cost fiber array assembly was presented by Arne Leinse in the framework of the new FP7 project PHASTFLEX, in which the low losses of TripleX enable the manufacturing of an interposer between an InP or Silicon Photonic PIC and the fiber array.

With regards to the Level 0 and Level 1 packaging, the optical interconnection of the above-mentioned technologies is in the roadmap of KIT, presented by Christian Koos, Head of the Institute IPQ and IMT, which is using the photonic bonding wire bonding solution. In a similar line, but from the commercial side, a competitive solution was presented by Markus Riester, CEO of Multiphoton Optics, based on 3D laser lithography by 3D patterning using a femtosecond laser inside a thin layer of material deposited on the top of the PIC.

The automation of the packaging of PICs for the volume manufacturing was presented by Ignazio Piacentini, Director of International Programs and PI miCos, and Torsten Vahrenkamp, CEO at ficonTEC. Mr Piacentini presented his company solutions for the 4 major ingredients in the automated assembly of PICs: subnanomechanics, machine vision, pick and place, and application specific software; a concept borrowed from the automatic industry. PI miCos automated system can assemble a few parts per hour today, and this throughput can be increased if more investment is made in improving the equipment. Torsten Vahrenkamp, focused his presentation on the need of standardization on the equipment for manufacturing. He concluded with a very interesting statement: customization constitutes 50% of the equipment price nowadays, thus standardization has the potential to significantly lower the equipment cost, and thus, the price of the assembly per unit.

Shall the PIC community work together towards some common packaging standards?

The above question was in fact the purpose of this workshop, and the audience was in a unique position not only to answer it but also to take the initial steps towards establishing a common ground. The workshop counted on his attendants with some of the key packaging experts and PIC users in the high and low volume applications. The low volume manufacturing of packaging for PICs was presented by Dario Lo Cascio, CEO at Technobis ipp. As of today, Technobis ipp provides low cost packaging solutions for the testing of PICs for the price of 3500 euros per unit, with a roadmap that can reduce this pricing by an order of magnitude in the coming years. In a similar line Bob Musk presented the packaging activities for InP PICs, with packages starting at 50 euros price per unit, which does not include the assembly of the components. In order to use the solutions above mentioned the designers have to use the design rules for the size and location of the electrical paths and IO interfaces. In order to facilitate the use of these design rules by the PIC designers, Twan Korthorst, CEO at Phoenix Software, presented the possibility of using existing libraries implemented in their design software offer. For the high volume packaging, Steffen Kroehnert, Director of Technology at Nanium, presented the fabrication facilities of the company based in Portugal.

Ronald Dekker, CTO at XiO Photonics, company with expertise of the manufacturing of products enabled by TripleX technology presented some of the challenges of the packaging of PICs. It was clear during his presentation as well as during the consequent discussion that currently there is a broad range of emerging applications realized in many different technologies but addressing very similar problems in terms of packaging. Therefore some form of standardization has to take place soon in order to keep PIC packaging economically feasible.

Many packaging standards exist, but which one to follow?

The workshop counted also with the expertise of the high volume market pullers of PIC technology, such as IBM and TE Connectivity. Bert Offrein, Manager of Photonics at IBM Research Zurich and Jeroen Duis, Technology Incubator and Manager of Photonics at TE Connectivity who lead a very interesting discussion on what path to follow in order to solve the above mentioned problem. The trend to close electro-optical integration for the high speed interconnects in the datacom market is one of the key aspects that enforces a first level packaging standardization, which will only be successful if there is a path to success for all contributors. In those lines, the presentation of Richard Pitwon, Lead Photonics Technology at Seagate, gave an overview of the achievements and future roadmap in their standardization work in the frameworks of association HDPUG and in the FP7 project PhoxTroT, in which they focus on the standardization activities of the optical circuit boards for data centres; those standardization activities are still in the early days. During his presentation, Mr. Pitwon encouraged the audience to contribute with their input to these activities.



To conclude, let's work together

All in all, it was a very interesting workshop full of content and plans for cooperation. Highlighted was the need for a common document in which the current and future packaging needs, the current de-facto and formal standards for the packaging of PICs both for testing as well for the low and high volume production would be included, as well as the roadmap for the customization of the test packages towards the commercial products. In order to put that into action a working group will be defined within the EPIC consortium. It is still too early to define this workshop as successful, as it will depend on the appropriate implementation of those action points. However what can indeed be concluded is that it was a very promising foundation of a stepping stones towards a healthy ecosystem for the packaging of PICs.



Extensive discussion, exchange, and networking takes place at every EPIC event.

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170 EPIC Members (1 June 2014)

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